IDEC Chip Design Contest

1/2/4 bit Reconfigurable BCH Decoder for Near-Threshold Voltage Operation

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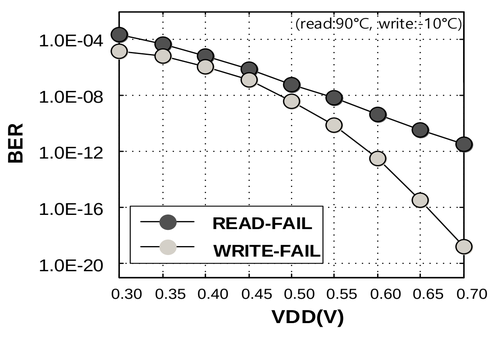
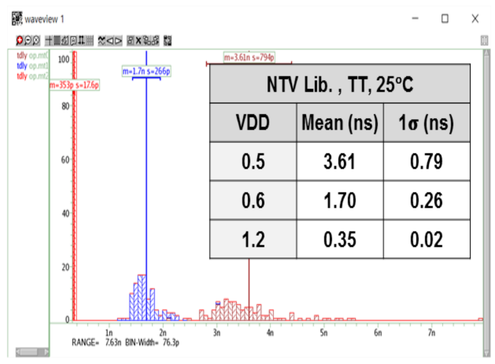
- Low delay reconfigurable BCH decoder for near-threshold voltage (NTV) operation is presented.
- Reconfigurable ECC which uses the scalable structure of BCH code is used, which is suitable for NTV environment.

Background

- **In near-threshold voltage (NTV) condition, there are several weaknesses compared to normal supply voltage condition, e.g. increase of BER or delay variation.**

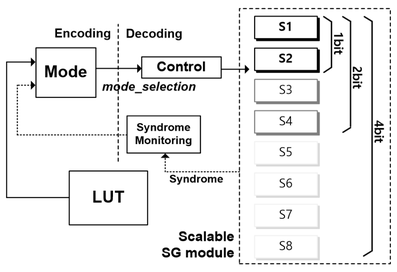


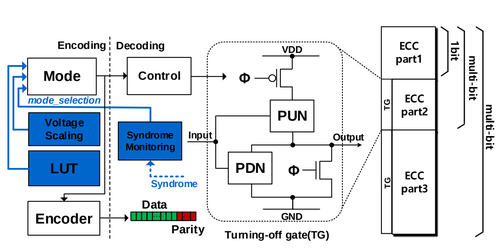
Bit error rate (BER) of the 6T SRAM raw cell according to the supply voltage and PVT variation

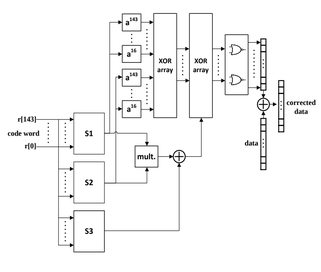


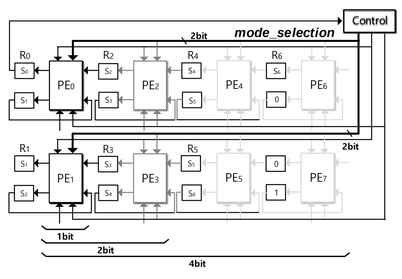
Delay variations of adder for various VDD

Main Contribution



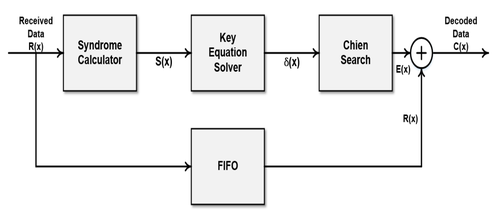




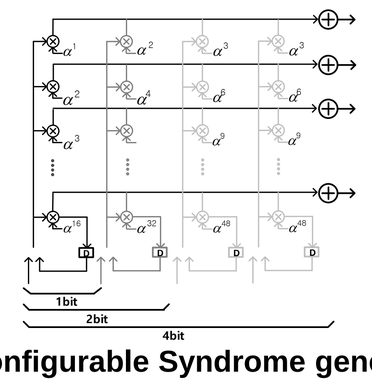


- **BCH decoder is implemented in reconfigurable structure to prevent excessive power consumption or delay – 1/2/4 bit error detectable**

Error Compensation for NTV Condition



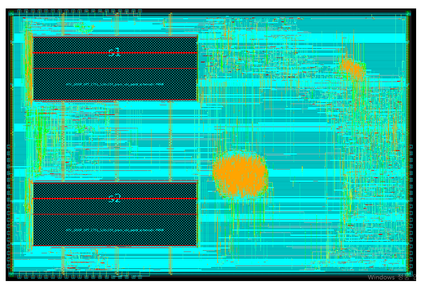
Binary BCH decoding process



Reconfigurable Syndrome generator

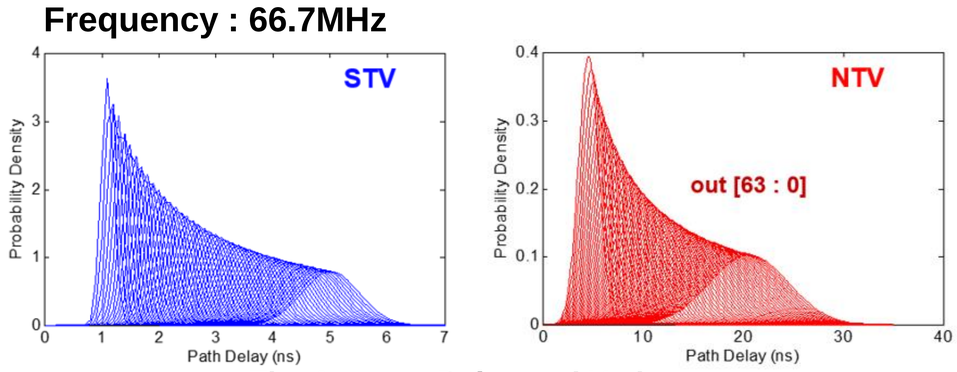
- **Implementing ECC hardware with scalable structure and error capability values in LUT can save the hardware cost and power consumption in NTV condition.**

Chip Implementation & Results



Samsung 65nm	Codeword	Area	Critical path	Power (mW)
4bit cor. BCH	160 bit	23161	6ns	3.82
Reconfi. BCH	136 bit	24850	6ns	3.96 (4bit)
	144 bit			2.26 (2bit)
	160 bit			1.46 (1bit)

- **Size : 1.5mm x 1.0mm (w/o pad) / 4.0mm x 4.0mm (w/ pad)**
- **Frequency : 66.7MHz**



The Average Delay and Variance

- **The average delay and variance increases by 4 ~ 5 times in NTV environment.**

- Proposed BCH decoder operates at 66.7MHz and achieve 3.2uW/MHz power efficiency.
- Test result showed 40.8% and 61.8% reduced power in case of 2bit and 1bit correction, compared to 4bit fixed BCH.